

May 24, 2001

Re: **09/379,985 (US 5,726,079)**

Dear Examiner Glick,

Attached are the requested litigation search results.

Several patent litigation and news databases were searched using Dialog, Lexis-Nexis and Questel-Orbit search systems.

**No** Litigation cases were found for this patent number.

Thank you for using EIC2800!

Paul Schulwitz  
308-6559  
CP4-9C18

**Schulwitz, Paul (Signal)**

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**From:** Glick, Ed  
**Sent:** Monday, May 21, 2001 4:39 PM  
**To:** STIC-EIC2800  
**Subject:** request for litigation search

Please perform a litigation search on US patent number 5,726,079 for placement in reissue application number 09/379,985.

Thanks

Ed Glick  
Special Programs Examiner TC-2800  
(703) 308-4858  
Ed.Glick@uspto.gov

1/39/1

DIALOG(R) File 345: ~~Impadoc/Fam. & Legal Stat~~  
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14211598

Basic Patent (No,Kind,Date): JP 10056103 A2 19980224 <No. of Patents: 005  
>

Patent Family:

Patent No	Kind	Date	Applic No	Kind	Date	
JP 10056103	A2	19980224	JP 97154889	A	19970612	(BASIC)
JP 3121562	B2	20010109	JP 97154889	A	19970612	
US 5726079	A	19980310	US 715212	A	19960917	
US 5883430	A	19990316	US 842417	A	19970424	
US 6104093	A	20000815	US 80117	A	19980515	

Priority Data (No,Kind,Date):

US 666155 A 19960619  
US 715212 A 19960917  
US 666155 B3 19960619  
US 842417 A 19970424  
US 715212 A3 19960917  
US 80117 A 19980515  
US 842417 A2 19970424

PATENT FAMILY:

JAPAN (JP)

Patent (No,Kind,Date): JP 10056103 A2 19980224  
FLIP CHIP PACKAGE AND ITS MANUFACTURING METHOD (English)  
Patent Assignee: IBM  
Author (Inventor): ERITSUKU AASAA JIYONSON  
Priority (No,Kind,Date): US 666155 A 19960619  
Applic (No,Kind,Date): JP 97154889 A 19970612  
IPC: \* H01L-023/12  
Derwent WPI Acc No: \* G 98-192781; G 99-214202  
Language of Document: Japanese  
Patent (No,Kind,Date): JP 3121562 B2 20010109  
Patent Assignee: IBM  
Author (Inventor): ERITSUKU AASAA JONSON  
Priority (No,Kind,Date): US 666155 A 19960619  
Applic (No,Kind,Date): JP 97154889 A 19970612  
IPC: \* H01L-023/12  
Language of Document: Japanese

UNITED STATES OF AMERICA (US)

Patent (No,Kind,Date): US 5726079 A 19980310  
THERMALLY ENHANCED FLIP CHIP PACKAGE AND METHOD OF FORMING (English)  
Patent Assignee: IBM (US)  
Author (Inventor): JOHNSON ERIC ARTHUR (US)  
Priority (No,Kind,Date): US 715212 A 19960917; US 666155 B3  
19960619  
Applic (No,Kind,Date): US 715212 A 19960917  
National Class: \* 438106000; 438108000; 438127000  
IPC: \* H01L-021/44  
Derwent WPI Acc No: \* G 98-192781; G 98-192781  
Language of Document: English  
Patent (No,Kind,Date): US 5883430 A 19990316  
THERMALLY ENHANCED FLIP CHIP PACKAGE (English)  
Patent Assignee: IBM (US)

Author (Inventor): JOHNSON ERIC ARTHUR (US)  
 Priority (No,Kind,Date): US 842417 A 19970424; US 715212 A3  
 19960917; US 666155 B3 19960619  
 Applic (No,Kind,Date): US 842417 A 19970424  
 Addnl Info: 5726079 19980310 Patented  
 National Class: \* 257706000; 257712000; 257720000; 257778000;  
 257796000  
 IPC: \* H01L-023/10; H01L-023/34; H01L-023/48; H01L-023/52  
 Derwent WPI Acc No: \* G 98-192781; G 99-214202; G 99-214202  
 Language of Document: English  
 Patent (No,Kind,Date): US 6104093 A 20000815  
 THERMALLY ENHANCED AND MECHANICALLY BALANCED FLIP CHIP PACKAGE AND  
 METHOD OF FORMING (English)  
 Patent Assignee: IBM (US)  
 Author (Inventor): CALETKA DAVID V (US); DERY JEAN (CA); DUCHESNE  
 ERIC (CA); GAYNES MICHAEL A (US); JOHNSON ERIC A (US); MATIENZO  
 LUIS J (US); WILCOX JAMES R (US)  
 Priority (No,Kind,Date): US 80117 A 19980515; US 842417 A2  
 19970424  
 Applic (No,Kind,Date): US 80117 A 19980515  
 Addnl Info: 5883430 Patented  
 National Class: \* 257778000; 257706000; 257737000  
 IPC: \* H01L-023/48  
 Derwent WPI Acc No: ; C 00-505551  
 Language of Document: English

UNITED STATES OF AMERICA (US)

Legal Status (No,Type,Date,Code,Text):

US 5726079	P	19960619	US AA	PRIORITY
			US 666155 B3	19960619
US 5726079	P	19960917	US AE	APPLICATION DATA (PATENT)
			(APPL. DATA (PATENT))	
			US 715212 A	19960917
US 5726079	P	19980310	US A	PATENT
US 5726079	P	19991026	US RF	REISSUE APPLICATION FILED
			(REISSUE APPL. FILED)	
			19990824	
US 5883430	P	19960619	US AA	PRIORITY
			US 666155 B3	19960619
US 5883430	P	19960917	US AA	PRIORITY
			US 715212 A3	19960917
US 5883430	P	19970424	US AE	APPLICATION DATA (PATENT)
			(APPL. DATA (PATENT))	
			US 842417 A	19970424
US 5883430	P	19990316	US A	PATENT
US 5883430	P	19990810	US CC	CERTIFICATE OF CORRECTION
US 6104093	P	19970424	US AA	PRIORITY
			US 842417 A2	19970424
US 6104093	P	19980515	US AE	APPLICATION DATA (PATENT)
			(APPL. DATA (PATENT))	
			US 80117 A	19980515
US 6104093	P	20000815	US A	PATENT

1/1 PLUSPAT - (C) QUESTEL-ORBIT

PN - US5726079 A 19980310 {US5726079}

TI - (A) Thermally enhanced flip chip package and method of forming

PA - (A) IBM (US)

IN - (A) JOHNSON ERIC ARTHUR (US)

AP - US71521296 19960917 [1996US-0715212]

PR - US66615596 19960619 [1996US-0666155]

- US71521296 19960917 [1996US-0715212]

IC - (A) H01L-021/44

EC - H01L-021/60C4

- H01L-023/31H2

- H01L-023/433E

PCL - ORIGINAL (O) : 438106000; CROSS-REFERENCE (X) : 438108000 438127000

DT - Basic

CT - US5289346; US5359768; US5405809; US5410451; US5471027; US5490324

STG - (A) United States patent

AB - A thermally conductive planar member is in thermally conductive communication with a flip chip encapsulated within a dielectric material that surrounds portions of the thermally conductive planar member, the flip-chip, and a predefined portion of a substrate member. The present invention provides a flip chip package having pick-and-place capability without the thermal resistance disadvantage of capped chip packages.

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1/1 LGST - (C) LEGSTAT

PN - US 5726079 {US5726079}

AP - US 715212/96 19960917 [1996US-0715212]

DT - US-P

ACT - 19960917 US/AE-A

APPLICATION DATA (PATENT)

{US 715212/96 19960917 [1996US-0715212]}

- 19980310 US/A

PATENT

- 19991026 US/RF

REISSUE APPLICATION FILED

19990824

UP - 1999-44

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1/1 CRXX - (C) CLAIMS/RXX

AN - 2951191

PN - 5,726,079 A 19980310 {US5726079}

PA - International Business Machines Corp

PT - C (Chemical)

ACT - 19990824 REISSUE REQUESTED

Issue Date of O.G.: 19991026

Reissue Request Number: 09/379985

Examination Group responsible for Reissue process: 2812

UP - 1999-42

UACT- 1999-10-26

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1/1 PAST - (C) PAST

AN - 199943-001333

PN - 5726079 A [US5726079]  
DT - A (UTILITY)  
OG - 1999-10-26  
CO - REA  
ACT - REISSUE APPLICATION FILED  
SH - REISSUE APPLICATION FILED

Source: All Sources : Area of Law - By Topic : Patent Law : Patents : U.S. Patents : Utility Patents 

Terms: patno is 5,726,079 (Edit Search)

Pat. No. 5726079, \*

~~5,726,079~~◆ GET 1st DRAWING SHEET OF 2

Mar. 10, 1998

Thermally enhanced flip chip package and method of forming

**REISSUE:** Reissue Application filed Aug. 24, 1999 (O.G. Oct. 26, 1999) Ex. Gp.: 2812; Re. S.N. 09/379,985**INVENTOR:** Johnson, Eric Arthur, Greene, New York**ASSIGNEE-AT-ISSUE:** International Business Machines Corporation, Armonk, New York (02)**APPL-NO:** 715,212**FILED:** Sep. 17, 1996**REL-US-DATA:**


Division of Ser. No. 666,155, Jun. 19, 1996 now abandoned

**INT-CL:** [6] H01L 21#44**US-CL:** 438#106; 438#108; 438#127**CL:** 438**SEARCH-FLD:** 437#209, 211, 214, 215, 217, 218, 219, 402**REF-CITED:****U.S. PATENT DOCUMENTS**

5,289,346	2/1994	* Carey et al.	437#209
5,359,768	11/1994	* Haley	437#209
5,405,809	4/1995	* Nakamura et al.	437#211
5,410,451	4/1995	* Hawthorne et al.	437#209
5,471,027	11/1995	* Call et al.	437#902
5,490,324	2/1996	* Newman	437#209

**PRIM-EXMR:** Picardat, Kevin**LEGAL-REP:** Mobley, Esq.; Michele A.  
Jenkins & Gilchrist, P.C.  
Tiegerman, Esq.; Bernard**CORE TERMS:** chip, flip, planar, thermally, conductive, substrate, package, mold, cavity, dielectric, thickness, electrical, predefined, embodying, thermal, upper surface, adhesive,

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us5,726,079

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